REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1, 2, 5-7, 9, 10, 13-17, and 19-28 are now in this application. Claims 1, 9, 17, and 22 have been amended. Claims 24-28 have been added to additionally and alternately claim the present invention.

The Examiner objected to the amendment filed on March 25, 2002 under 35 U.S.C. §132 as introducing new matter. The Examiner also rejected claims 1, 2, 5-7, 9, 10, and 13-17 under 35 U.S.C. §112, first paragraph. In both cases, the Examiner objected to the addition of the phrase "without changing the slurry," arguing that there is no support in the specification for this limitation. Although applicant disagrees with the argument set forth by the Examiner, applicant has removed the phrase "without changing the slurry" from claim 1 to further prosecution. As a result, the amendment to claim 1 is believed to remove the section 132 objection. In addition, claims 1, 2, 5-7, 9, 10, and 13-17 are believed to satisfy the requirements of the first paragraph of section 112.

The Examiner rejected claim 20 under 35 U.S.C. §112, first paragraph. Specifically, the Examiner argued that the phrase "wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal or greater than the minimum thickness" is not supported by the specification. Applicant notes that claim 20 was amended in a previous response, and no longer recites the language quoted by the Examiner. As a result, claim 20 is believed to satisfy the requirements of the first paragraph of section 112.

The Examiner also rejected claims 5, 13, and 20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant addressed this rejection in the amendment filed on November 1, 2002 and, from applicant can determine, the Examiner has not responded to these arguments. As a result, applicant re-presents the remarks presented in the previous amendment.

Claims 5 and 13 are similar to claim 20, and recite, in part,

> "wherein the planarized layer of material has a thickness over the wafer upper level, and

"wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness."

In rejecting the claims, the Examiner argued that the "wherein the layer of first material" phrase lacks clarity.

Applicant's specification teaches:

"When the structures are formed, the structures are specified to have a thickness over the upper levels 314 that ranges from a minimum thickness to a maximum thickness. To achieve this result, polysilicon layer 320 is deposited to have a thickness such that lower level 322 is above upper level 314 by an amount which is at least as great as the minimum specified thickness of the resulting structure." (See page 6, lines 4-9.)

The layer of first material can be read to be, for example, polysilicon layer 320, while the first lower level can be read to be, for example, a lower level 322. In addition, the wafer upper level can be read to be, for example, an upper level 314, while the thickness can be read to be, for example, the minimum specified thickness. (See also the example on page 6, lines 10-19 of applicant's specification.) Thus, from what applicant can determine, claims 5, 13, and 20 satisfy the requirements of the second paragraph of section 112.

The Examiner rejected claims 1, 2, 6, 7, and 14-16 under 35 U.S.C. §102(b) as being anticipated by Doan et al. (U.S. Patent No. 5,618,381). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 has been amended and recites, in part,

"chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level."

Thus, claim 1 requires that the polishing step stop when the layer of second material is substantially all removed from the layer of first material, and form a planarized layer of material so that the planarized layer of material lies over the wafer upper levels and the wafer lower level. (The location of the planarized layer of material was added to more precisely define the location. The term substantially was added to broaden the claim.)

In rejecting the claims, the Examiner pointed to the formation of tungsten layer 22 shown in FIG. 6 of Doan as constituting the step of "forming a layer of first material" required by claim 1, and the formation of TEOS layer 60 as constituting the step of "forming a layer of second material" required by claim 1. The Examiner also pointed to the step of planarizing tungsten layer 22 as constituting the chemically-mechanically polishing step of claim 1.

The Doan reference, however, fails to teach that a planarized layer of material lies over the wafer upper levels and the wafer lower level when the polishing step stops. As taught by Doan, the most protruding areas of TEOS layer 60 are removed with a first CMP process which, as shown in FIG. 7, results in areas of bare tungsten 70 and areas of tungsten layer 22 that remain covered with TEOS layer 60. (See also column 4, lines 14-21 of Doan.) However, regardless of whether TEOS layer 60 has been substantially all removed or not, FIG. 7 of Doan does not show a planarized layer of material that lies over the wafer upper levels and the wafer lower level. Thus, at the end of the first CMP process, Doan fails to teach the limitations of claim 1.

Doan also teaches a second CMP process where tungsten layer 22 and the remaining TEOS layers 60 are etched, thereby leaving the structure as shown in FIG. 3. (See also column 4, lines 36-38 of Doan.) Comparing FIGs. 3 and 7 of Doan shows that when the second polishing step has ended, a planarized layer of material still does not lie over the wafer upper levels and the wafer lower level.

Thus, since the Doan reference does not teach that a planarized layer of material lies over the wafer upper levels and the wafer lower level when the polishing step stops, claim 1 is not anticipated by Doan. In addition, since claims 2, 6, 7, and 14-16 depend either directly or indirectly from claim 1, claims 2, 6, 7, and 14-16 are not anticipated by Doan for the same reasons as claim 1.

The Examiner also rejected claims 1, 2, 5-7, 10, 13-16, and 19-23 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,162,368). (Claim 18 was previously cancelled.) For the reasons set forth below, applicant respectfully traverses this rejection.

In rejecting claim 1, the Examiner pointed to polysilicon layer 16 shown in FIG. 2A of Li as constituting the layer of first material, and oxide layer 18 as constituting the layer of

second material. The Examiner also pointed to the step of planarizing polysilicon layer 16 as constituting the chemically-mechanically polishing step of claim 1.

The Li reference, however, fails to teach that the polishing step stops when oxide layer 18 (the layer of second material) has substantially all been removed. As taught by Li, "[t]he oxide polishing may occur only during the "ramp-up" period at the start of the polishing operation." (See column 5, lines 23-25 of Li.)

As a result, the Li reference does not teach that the polishing step stops when oxide layer 18 has been substantially all removed, but instead teaches that oxide layer 18 is removed at the beginning of a polishing step that continues with the planarization of polysilicon layer 16 until the structure shown in FIG. 2D has been formed. Thus, since Li does not teach that the polishing step stops when oxide layer 18 has substantially all been removed, claim 1 is not anticipated by the Li reference. In addition, since claims 2, 5-7, 10, and 13-16 depend either directly or indirectly from claim 1, claims 2, 5-7, 10, and 13-16 are also not anticipated by the Li reference.

With respect to claim 22, claim 22 has been amended to recite, in part,

> "forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material."

In rejecting the claims, the Examiner stated that Li discloses "all of the claimed limitations including the limitation forming of a third layer of material formed over the planarized layer of the first material (see FIG. 2D)." (See page 14 of the office action.) The Examiner, however, did not identify the structure that the Examiner read to be the third layer of material. As a result, applicant is unclear as to the structure the Examiner is reading to be the third layer of material.

As shown in FIG. 2D, Li shows a polishing slurry 50b placed between polishing pad 100 and polysilicon layer 16. Thus, applicant assumes the Examiner is reading slurry 50b to be the layer of third material. To further clarify claim 22, claim 22 has been amended to recite that the third layer of material lowers the resistance of the first layer of material. From what applicant can tell, slurry 50b does not lower the resistance of polysilicon layer 16. Thus, since slurry 50b does not lower the resistance of polysilicon layer 16, claim 22 is not

anticipated by Li. In addition, since claims 19, 21, and 23 depend from claim 22, claims 19, 21, and 23 are not anticipated by Li for the same reasons as claim 22.

The Examiner also rejected claims 9 and 17 under 35 U.S.C. §103(a) as being unpatentable over Li et al. From what applicant can determine, there is no discussion in Li that teaches or suggests stopping the polishing step when substantially all of the layer of second material has been removed. Thus, claim 1 is patentable over Li. In addition, since claims 9 and 17 depend either directly or indirectly from claim 1, claims 9 and 17 are patentable over Li for the same reasons as claim 1.

With further respect to claim 17, claim 17 has been amended to recite that "the second layer of material is thicker than the layer of first material." The Examiner appears to argue that the claimed limitation is obvious because determining an optimum thickness is a matter of routine experimentation. In this case, however, applicant has been unable to find any discussion that teaches or suggests that the optimal thickness of oxide layer 18 would ever be thicker than polysilicon layer 16. The issue is not whether one skilled in the art would understand that the second layer could be formed to be thicker than the first layer. Rather, the issue is what would motivate one skilled in the art to make the second layer thicker than the first layer.

From what applicant can tell, the Li reference teaches away from increasing the thickness of oxide layer 18. As taught by Li, "native oxide layer 18 interferes with the polishing of the polysilicon layer 16." (See column 4, lines 66-67 of Li.) Since oxide layer 18 interferes with the polishing, one skilled in the art would not be motivated to substantially increase the thickness of oxide layer 18 so that oxide layer 18 is greater than the thickness of polysilicon layer 16. As a result, claim 17 is patentable over the Li reference for this additional reason.

With respect to new claim 24, claim 24 recites, in part,

> "chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of material, the planarized layer of material covering the wafer upper levels and the wafer lower level of the top surface of the wafer; and
>
> "selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer.

Applicant has been unable to find any discussion in Li that teaches or suggests that polysilicon layer 16 (read to be the layer of first material) is selectively etched when polysilicon layer 16 covers the upper levels of regions 14 as required by claim 24. As a result, new claim 24 is patentable over Li. In addition, since claims 25-28 depend either directly or indirectly from claim 24, claims 25-28 are patentable over Li for the same reasons as claim 24.

Similarly, applicant has been unable to find any discussion in Doan that teaches or suggests that tungsten layer 22 (read to be the layer of first material) is selectively etched when tungsten layer 22 covers the upper level of regions 10 as required by claim 24. As a result, new claim 24 is patentable over Doan. In addition, since claims 25-28 depend either directly or indirectly from claim 24, claims 25-28 are patentable over Doan for the same reasons as claim 24.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

Dated: 3-4-03 By: _____

Mark C. Pickering
Registration No. 36,239

Attorney for Assignee

P.O. Box 300
Petaluma, CA 94953-0300
Direct Dial Telephone No. (707) 762-5583
Telephone: (707) 762-5500
Facsimile: (707) 762-5504

APPENDIX

In the Claims

Please amend the claims as follows:

1. (Twice Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level [and a wafer upper level] that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material [without changing the slurry] to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

9. (Amended) The method of claim 1 wherein the [first and second layers of material are chemically-mechanically polished with a] slurry [that] has a selectivity that falls within an approximate range of 0.9-1.1:1.

17. (Amended) The method of claim 1 wherein the second layer of material is [approximately two to three times as thick as] thicker than the layer of first material.

22. (Twice Amended) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material.

New claims 24-28 have been added.